Asymmetry Half Bridge Soft-Switching PFC Converter with Direct Energy Transfer

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Abstract: ***A single stage power factor correction AC/DC converter with direct energy transfer branch is proposed in this paper. Asymmetric Half-Bridge was used as a DC-DC cell for its inherent ZVS capability, a direct energy transfer transformer which replaces the conventional boost inductor is introduced to further improve the efficiency.***

I. INTRODUCTION

For years a great deal of effort has been made to develop efficient and cost-effective power factor correction (PFC) schemes to meet the tight regulation standards such as IEC 1000-3-2. Active PFC techniques include the conventional two-stage and single-stage configurations have been addressed strongly in the open literature. Between the two schemes the single-stage configuration receives particular attention in low power applications because of its low cost and simple implementation [1,2].

Efficiency of the single-stage converter is what the industry demands nowadays. To improve the efficiency Figure 1, illustrats the general configuration of the proposed converter where the idea about parallel energy transfer introduced in [3-5] adopted here to directly transfer a portion of the input power to the output with simple implementation and without the need to process the power twice through the PFC and the DC/DC cells, and hence avoid the penalty of the conduction and switching losses on the efficiency. As can be seen in Figure 1, the proposed single stage converter uses PFC cell that operates in DCM to achieve power factor correction in a natural manner. Asymmetric Half-bridge converter (AHBC) is used at the output side for regulation. In addition to the tight output regulation, AHBC is distinct from other soft switching converters by its inherent ZVS capabilities where ZVS can be achieved for booth switches by allowing small dead-time between the switching so that the energy stored in the leakage inductor of the main transformer can resonate with the switches parasitic capacitance [2]. Moreover, AHBC do not have to sacrifice the low conduction losses of the conventional hard switching converters to eliminate the switching losses using soft switching [5].

In this paper, a single-stage soft switching power factor correction circuit is proposed to achieve high efficiency with low implementation cost. The principle of operation and the steady state analysis are presented along with simulation and some experimental results for 150W @ 200KHz.

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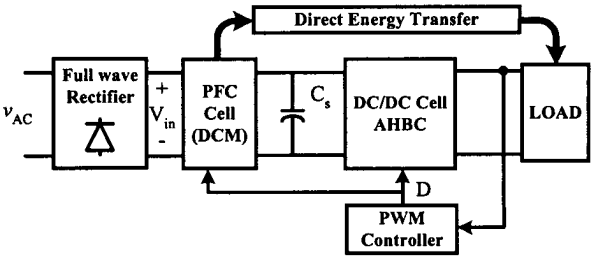


Fig. 1: General configuration of the proposed single stage converter

II. PROPOSED CONVERTER AND ITS OPERATION

The proposed soft-switching converter in Figure 2 is obtained simply by adding a flyback transformer to the existing DC-DC AHBC. Diodes D_{PF} and D_{SF} will provide the flyback operation during the other portion of the rectified ac input voltage to transfer the energy directly to the output. The bulk capacitor C_s will store energy from PFC cell and deliver it to the forward configuration of the AHBC. The asymmetric capacitor C_a will balance the Asymmetry operation in the output side. It can be shown that the FPC cell operates in two different regions, flyback region and boost region, during one line cycle as shown in Figure 3(a).

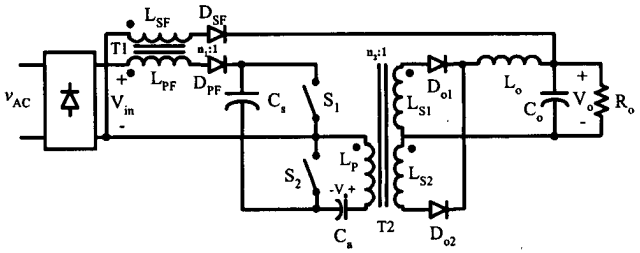


Fig. 2: Proposed Topology

The following assumptions have been made throughout the steady state analyses:

- V_o is constant during the line cycle.
- V_{in} is the average rectified ac input during one switching cycle and its value is a moving average that will vary with time over the line cycle.
- The dead time between the switches conduction is negligible.
- The leakage inductance of the transforms and the parasitics of the switches will be ignored, since it affects just the resonant period during the dead time.

- The capacitors *Cs* and *Ca* are large enough so that the voltage ripple across each is negligible.

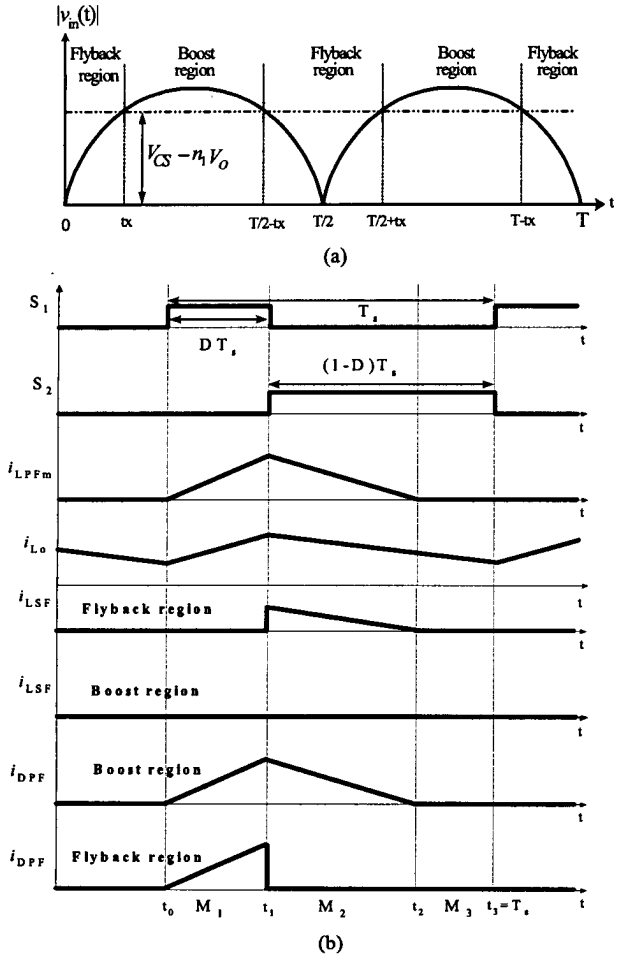


Fig. 3 (a) Regions of Operation, (b) Operation Waveforms

The modes of operation are discussed as follows:

Mode 1 [t_o<t<t_1]:

At t=t_o, S1 will turn *ON* and so do D_{PF}. V_{in} is applied to the magnetizing inductor L_{PFm} causing the DCM current to increase linearly. The difference between the storage and the asymmetric capacitors voltage will be applied to the primary side of T2 causing L_{Pm} to charge linearly. S1 will turn *OFF* At t=t_1. The equivalent circuit during this mode is shown in Fig. 4(a).

Mode 2 [t_1<t<t_2]:

I) FlyBack region: For $|v_{in}(t)| < V_{Cs} - n_1 V_o$

At t=t_1, S2 and D_{PF} will turn *ON* so that the magnetizing current in L_{PFm} will be discharged to the secondary winding and the energy stored will be transferred to the output. D_{PF} blocks the current from charging through the storage capacitor. The negative voltage of C_a will be applied to the primary of T2 discharging the output inductor L_o. The period ends when the magnetizing inductor current, i_{PFm}, reaches zero at t_2. The equivalent circuit during this mode is shown in Fig. 4(b)

II) Boost region: For $|v_{in}(t)| > V_{Cs} - n_1 V_o$

In this region, S2 turns *ON* but D_{PF} will keep *ON* and D_{SF} *OFF* due to the region condition. The energy stored in the magnetizing inductor L_{PFm} will be released to charge C_s. Meanwhile the negative voltage of C_a will discharge the output and T2 magnetizing inductors. This mode ends when the magnetizing inductor current, i_{PFm}, reaches zero at t_2. The same equations for i_{LPm} and i_{Lo} from mode 2 in the flyback region can be applied here. The equivalent circuit is shown in Fig. 4(c).

Mode 3 [t_2<t<t_3]

The current i_{LSF} stays zero in this mode. The output current will continue discharging along with i_{Lpm} until S2 turns *OFF* again. The same equations for i_{LPm} and i_{Lo} from mode 2 can be applied here.

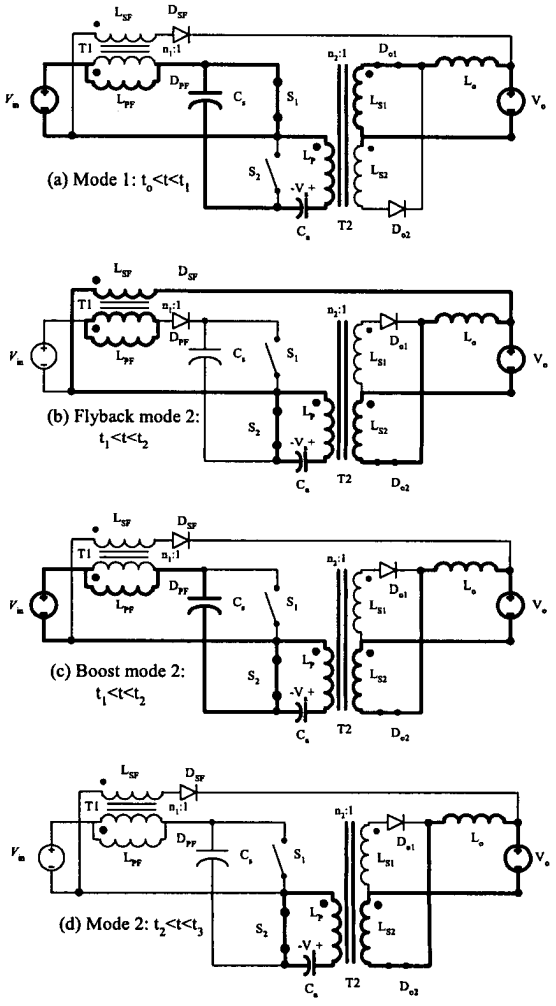


Fig. 4 Equivalent circuit modes

III. STEADY-STATE ANALYSIS

A. Region boundary

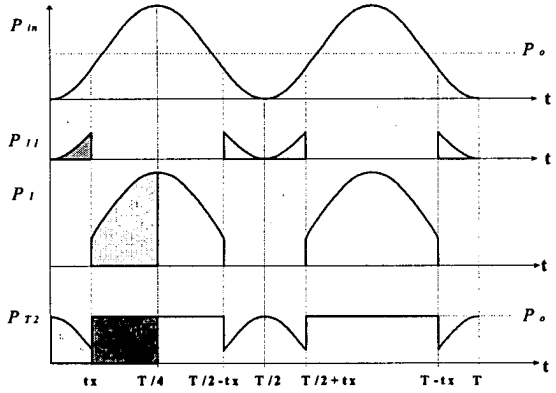
Based on the operation analysis in last section, the boundary time for the two regions is given by:

$$t_x = \frac{1}{\omega}\sin^{-1}\left(\frac{V_{cs} - n_1 V_o}{V_p}\right) \quad (1)$$

where

$$v_{in}(t) = V_p \sin(\omega t) \quad (2)$$

B. Stead-state equation for intermediate bus voltage



Pin: Input power
P11: Power transferred by T1 at flyback mode
P1: Power transferred by T1 at boost mode
P2: Power delivered by T2

Fig. 5 Power flow over a line period

Since the operation of the proposed topology is symmetrical, only operation in the first quarter of line period needs to be analyzed.

The DC/DC conversion cell of the proposed topology is a typical Asymmetric Half Bridge topology. When it operates in CCM, the duty cycle should be constant for the entire line period to achieve tight output regulation. The DC/DC conversion cell gain is given by:

$$\frac{V_o}{V_{cs}} = \frac{2D(1-D)}{n_2} \quad (3)$$

During the flyback region (0 ~ t_x), in a given switching cycle, transformer T1 is charged by the rectified input voltage and completely discharged to the load.

The average power transferred directly to the load through T1 during one switching cycle is given by,

$$P_{T1} = \frac{V_{in}^2 D^2 T_s}{2L_{PFm}} \quad (4)$$

In order to keep tight output voltage regulation, i.e. V_o constant, the total power delivered directly through T1 and by the storage capacitors through T2 should be equal to output power in each switching cycle during the flyback region. Hence the power delivered by T2 in one switching cycle is,

$$P_{T2} = P_o - P_{T1} = P_o - \frac{V_{in}^2 D^2 T_s}{2L_{PFm}} \quad (5)$$

The total power from intermediate bus capacitor during flyback mode (0~t_x) is given by,

$$P_{T2,Flyback} = \sum_{t=0,T_s,2T_s,\ldots}^{t_x} P_{T2} \quad (6)$$

Since the switching frequency is much higher than line frequency $T_s << T$, V_{in} is Eq. (5) can be replaced by $v_{in}(t)$ and the summation in Eq. (6) can be converted to following integration,

$$P_{T2,Flyback} = \frac{1}{t_x}\int_0^{t_x} P_{T2}dt = \frac{1}{t_x}\int_0^{t_x}\left(\frac{V_o}{R_L} - \frac{D^2 T_s}{2L_{PFm}} v_{in}(t)^2\right)dt \quad (7)$$

In the boost region (t_x~T/4), all the energy charged by the input transformer is transferred to the storage capacitors to recover its loss in the flyback region.

The average power transferred through T1 during one switching cycle is given by,

$$P_{T1} = V_{in} I_{in,avg} = \frac{D^2 T_s}{2L_{PFm}} \frac{V_{cs} V_{in}^2}{V_{cs} - V_{in}} \quad (8)$$

As in Eqs. (6, 7) the average input power during boost region (t_x ~ T/4), is given by,

$$P_{T1,boost} = \frac{1}{T/4 - 2t_x}\int_{t_x}^{\frac{T}{4}} P_{T1}dt = \frac{1}{T/4 - 2t_x}\int_{t_x}^{\frac{T}{4}} \frac{D^2 T_s}{2L_{PFm}} \frac{V_{cs} v_{in}(t)^2}{V_{cs} - v_{in}(t)}dt \quad (9)$$

And the average power directly transferred to load by T2 during boost region is:

$$P_{T2,boost} = P_o = \frac{V_o}{R_L} \quad (10)$$

In steady state, the voltage across the intermediate bus capacitor is constant; then from Figure 5 we can write the general equation for study as,

$$\left(P_{T1,boost} - P_{T2,boost}\right)\left(\frac{T}{4} - t_x\right) = P_{2,Flyback}(tx) \quad (11)$$

Substituting Eqs. (7, 9, and 10) in Eq. (11) yields,

$$\frac{V_{cs} D^2 T_s}{2L_{PFm}}\int_{t_x}^{\frac{T}{4}} \frac{v_{in}(t)^2}{V_{cs} - v_{in}(t)}dt = \frac{V_o T}{4R_L} - \frac{V_p^2 D^2 T_s}{2L_{PFm}}\left(\frac{t_x}{2} - \frac{\sin(2\omega t_x)}{4\omega}\right) \quad (12)$$

Eqs. (1, 2, 3 and 12) show the relationship between intermediate bus voltage and other circuit parameters. It is a transcendental equation that can be solved by mathematical software, such as MathCAD©.

C. Condition for PFC cell in DCM

In order to keep PFC cell in DCM, we can obtain the following condition for D:

$$D \le \frac{V_{cs} - V_P}{V_{cs}} \quad (13)$$

Also the intermediate bus voltage should always satisfy the following condition,

$$V_{cs} \le V_P + n_1 V_o \quad (14)$$

IV. COMPUTER SIMULATION &EXPERIMENTAL RESULTS

A 150W @ 200KHz with 28V output circuit was simulated in Pspice using the following values: L_{PFm}=12μH, L_{Pm}=2mH, L_o=10μH, C_s=470μF, C_a=2.2μF, n_1=4.5, n_2=3. The close loop simulation results over one line cycle are given in Figure 6. It is clear from the figure that the input current is following the line voltage, which promises high power factor.

Figures 7, 8 show the experimental results obtained from prototyping the simulated circuit to verify its operation. Experimental waveforms of input current and voltage are shown in Figure 7. The measured Power Factor was 0.986. Figure 8 shows an efficiency of about 84% for 150W@28V output operating at 200KHz, which is a significant improvement over the old AHBC.

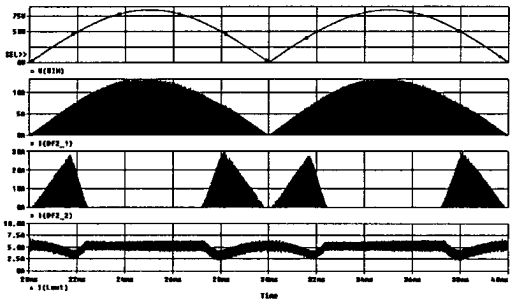


Fig. 6 Simulation waveforms for one line cycle

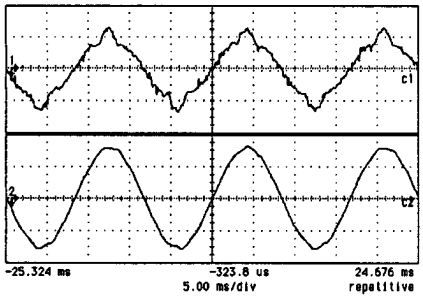


Fig. 7 line current (upper trace) and Line voltage (lower trace).

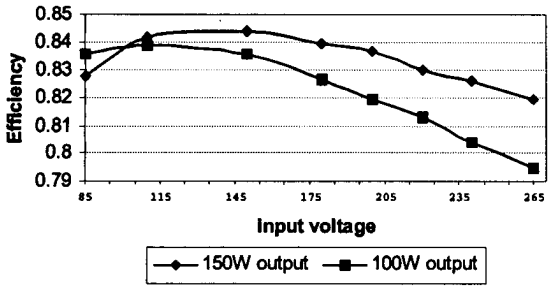


Fig. 8 Efficiency versus Line voltage

V. CONCLUSION

An improved Asymmetric Half-Bridge Soft-Switching PFC Converter was introduced in this paper. By replacing the boost inductor with flyback transformer, the energy can be directly delivered to the output during low line voltage. The simple implementation and the high efficiency of the proposed converter promises commercial advantage while the selected cells topologies will provide high quality performance in terms of PFC and output regulation. Steady state analysis shows that there exist three modes of operation either in the flyback or boost regions. Experimental results proved the improvement in efficiency and high PFC was achieved. The proposed converter is believed to be a high competitor in today's single stage PFC power supplies.

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